

IN THE CLAIMS

Claim 1 (Currently Amended): A semiconductor device ~~with a CMOS transistor~~
comprising:

plural CMOS transistors comprising,

first and second transistors sharing a common first gate electrode and third and
fourth transistors sharing a common second gate electrode that is adjacent and parallel
to the first gate electrode, said first and third transistors sharing a common n-type
channel MOS region and said second and fourth transistors sharing a common p-type
channel MOS region;

~~a plurality of gate electrodes arranged in parallel with one another;~~

~~an n-channel MOS region and a p-channel MOS region of said CMOS transistor~~
~~which are arranged adjacent to each other in a lengthwise direction of said plurality of gate~~
~~electrodes; and~~

a wire ~~[[for]]~~ connecting said ~~n-channel~~ n-type channel MOS region and said ~~p-~~
~~channel~~ p-type channel MOS region,

wherein said wire has a width greater than a distance between ~~every two adjacent ones~~
~~of said plurality of~~ said first and second adjacent gate electrodes, and

a portion of said wire is disposed right above a portion of ~~[[said]]~~ at least one of the
first and second gate electrode electrodes with an insulating film interposed therebetween.

Claim 2 (Original): The semiconductor device according to claim 1,

wherein said insulating film is formed on a top face and a side face of said gate
electrode, and

said wire is buried in a first opening formed by carrying out etching on an interlayer insulating film which is deposited on said insulating film and is made of a material different from a material for said insulating film.

Claim 3 (Original): The semiconductor device according to claim 2,
wherein said wire is further buried in a second opening formed in said insulating film,
to be electrically connected to said gate electrode.

Claim 4 (Original): The semiconductor device according to claim 3,
wherein said first opening and said second opening form one opening which provides
a shape having six corners or more in said interlayer insulating film in plan view.

Claim 5 (Withdrawn): A method of manufacturing a semiconductor device with a
CMOS transistor, comprising the steps of:

forming a plurality of gate electrodes so as to be arranged in parallel with one another
on a semiconductor substrate;

forming an insulating film on a top face and a side face of said gate electrode;

forming an interlayer insulating film made of a material different from a material for
said insulating film, on said insulating film;

carrying out etching on said interlayer insulating film using said insulating film as an
etch stop layer, to form a first opening having a width greater than a distance between every
two adjacent ones of said plurality of gate electrodes;

depositing a metal film on said interlayer insulating film; and

removing said metal film on said interlayer insulating film, except a portion of said
metal film which is buried in said first opening.

Claim 6 (Withdrawn): The method of manufacturing a semiconductor device according to claim 5, further comprising a step of:

etching a portion of said insulating film which is exposed after said first opening is formed, to form a second opening.

Claim 7 (Withdrawn): The method of manufacturing a semiconductor device according to claim 5,

wherein said metal film on said interlayer insulating film except said portion of said metal film which is buried in said first opening is removed by etch back.

Claim 8 (New): A semiconductor device comprising:

first and second transistors sharing a common first gate electrode and third and fourth transistors sharing a common second gate electrode that is adjacent and parallel to the first gate electrode, said first and third transistors sharing a common n-type region and said second and fourth transistors sharing a common p-type region;

a first insulating film formed on said first gate electrode and a second insulating film formed on said second gate electrode;

a third insulating film formed on a side surface of said first electrode and a side surface of said first insulating film, and a fourth insulating film formed on a side surface of said second gate electrode and a side surface of said second insulating film;

an interlayer insulating film formed over and between said first and said second gate electrodes, and having an opening exposing said third and fourth insulating films and said first and second insulating films located between said first and said second electrodes, wherein said opening is located above said common n-type region and said common p-type region; and

a buried wiring formed in said opening and not extending over said interlayer insulating film, wherein said buried wiring extends above said first insulating film and said second insulating film.

Claim 9 (New): A semiconductor device according to claim 8, wherein said first, second, third and fourth insulating films are made of a material different from said interlayer insulating film.

Claim 10 (New): A semiconductor device according to claim 9, wherein said buried wiring is electrically connected to said common n-type region and said common p-type region.

Claim 11 (New): A semiconductor device comprising:
a semiconductor substrate;
first and second gate electrodes formed over said semiconductor substrate;
p-type regions located at both sides of said first gate electrode;
n-type regions located at both sides of said second gate electrode;
a first insulating film formed on said first gate electrode and a second insulating film formed on said second gate electrode;
a third insulating film formed on a side surface of said first gate electrode and a side surface of said first insulating film, and a fourth insulating film formed on a side surface of said second gate electrode and a side surface of said second insulating film;
an interlayer insulating film formed over and between said first and said second gate electrodes, and having an opening exposing said third and fourth insulating films and said first and second insulating films located between said first and said second electrodes,

wherein said opening is located above said one of p-type regions and said second gate electrode; and

a buried wiring formed in said opening and not extending over said interlayer insulating film,

wherein said buried wiring extends above said first insulating film formed over said first gate electrode and extends above said second insulating film formed over said second gate electrode, and

wherein said one of p-type region is electrically connected to said second gate electrode via said buried wiring.

Claim 12 (New): A semiconductor device according to claim 11, wherein said first, second, third and fourth insulating films are made of a material different from said interlayer insulating film.